8th Int. Symp. "Nanostructures: Physics and Technology"
St Petersburg, Russia, June 19–23, 2000

New prospects for terabit-scale integration

Konstantin K. Likharev
State University of New York, Stony Brook, NY 11794-3800, U.S.A.

Abstract. I will review several recent new ideas in the field of nanoelectronics that may eventually revolutionize the semiconductor memory and data storage technologies.

Crested barriers

The electronics industry predicts [1] that the current progress in scaling down silicon MOSFETs will lead eventually to gigabit-scale electronic circuits, most importantly, dynamic random-access memories (DRAM) with density of the order of 5 Gbits/cm^2 and integration scale up to 64 Gbits per die. Further evolution in this direction is, however, very much in doubt: though silicon field-effect transistors may apparently be scaled down to sub-10-nm channel lengths [2, 3], DRAM storage capacitors are non-scalable since their capacitance has to be large enough to charge the output lines all the way down to sense amplifiers. On the other hand, floating-gate cells of nonvolatile memories [4] are scalable, but their write/erase times are so slow (of the order of 1 microsecond) that they cannot serve as a basis for mainstream, bit-addressable memories.

The situation may be changed by the recently proposed [5, 6] "crested" tunnel barriers, with an electrostatic potential peaking in the middle. In these barriers, applied voltage increases the barrier transparency much more quickly than in usual uniform (say, SiO_2) barriers. Calculations have shown that crested barriers may combine a sufficiently long retention time (above 10 years) with fast write/erase time (below 10 nanoseconds). This performance may be reached at low electric fields (below 10 MV/cm), promising high barrier endurance under electric stress. In addition, low write/erase fields limit disturb effects and as a result allow the simplest floating gate memory architectures to be used, increasing circuit density.

NOVORAM

This radical improvement may be used, first of all, for the development of fast nonvolatile random-access memories (NOVORAM) [5]. The NOVORAM cell structure is similar to that of the usual floating-gate memories, except that it uses Fowler-Nordheim tunneling through a crested barrier for both write and erase operations. Estimates show that NOVORAM may be denser than DRAM even at the current (few-100-nm) patterning technology level, adding the convenience of non-volatility.

Moreover, the incorporation of nanoscale MOSFETs with ballistic electron transfer along undoped channels [2, 3] may allow NOVORAM cells to be scaled down to a minimum feature size about 10 nm, corresponding to a memory density of about 100 Gbits/cm^2, and integration scale up to 16 Tbits per die [7, 6].

Single-electron memories

The NOVORAM scaling limit mentioned above is determined by MOSFET scaling [2, 3] and may be overcome by replacing field-effect transistors with single-electron transistors (SET). The fundamental effect of background charge randomness which hounds single-electron devices [7] may be circumvented in memories using either the so-called "SET/FET hybrids" with dynamic SET read-out in background-charge-insensitive mode [8, 9], or purely single-electron memories equipped with "nanofuses" [10] to exclude cells with inappropriate background charge values [11].

Estimates show that single-electron memories may be scaled down to at least 3 nm minimum feature size, enabling density beyond 1 Tbit/cm^2 and integration scale of at least 64 Tbits. If equipped with crested tunnel barriers, they may apparently sustain bit-addressable applications.

ESTOR

Crested barriers may also be used in the "ESTOR", a system for electrostatic data storage [12, 5]. In this system, a read/write head (tip) is flown over a substrate (disk) on which the crested barrier separates a conducting ground layer from a layer of nanometer-size metallic grains, not necessarily all of the same size or shape. The binary unity is coded by the few-electron charging of a small group of grains. Write/erase operation is achieved by the application of a sufficiently high voltage to the circuit on the tip. The recorded data may be read out by the activation of the single-electron transistor which is located on the tip. The SET output signal is further amplified by a closely located, FET-based sense amplifier and then sent out. Recent experiments by a Bell Labs group [13] may be considered as the first step toward the implementation of such readout.

Preliminary estimates show that electrostatic recording may provide data storage density about 1 Tbits/in^2, i.e., about two orders of magnitude higher than the presently demonstrated level, and an order of magnitude higher than the apparent fundamental limit, of magnetic recording density, if the read/write head can be flown at a comparable height (of the order of 15 nm) above the substrate surface. In contrast to earlier approaches to electrostatic data recording, the use of crested tunnel barriers may make possible a write/read speed up to 1 Gbps per channel, which seems adequate even for this unparalleled bit density.

Conclusion

It seems that the implementation of NOVORAM may revolutionize fast semiconductor memories, while ESTOR may play a similar role in the field of digital data storage, in the very near future. (Single-electron memories require a-few-nm patterning of VLSI scale, and shall take much more time to implement.) Moreover, if combined with the ultrafast superconductor-based RSFQ logic [14, 15], they may allow to develop affordable desktop-size teraflops-scale computers [16] within the next decade.

In my talk at the meeting I will describe these exciting opportunities in detail.

Acknowledgments

Important contributions of Alexander Korotkov, Yehuda Naveh, and Fedor Pikus are gratefully acknowledged. This work was supported by the Ultra Electronics and Advanced Microelectronics programs of DARPA (via ONR), and by the Nanostructures and Integration Sciences (NIS) Innovative Concepts Initiation Program of the Semiconductor Research Corporation.

References

[1] *International Technology Roadmap for Semiconductors, 1997 Edition/1998 Update* Semiconductor Industry Association, San Jose, CA, available on the Web at www.semichips.org.

[2] F. Pikus and K. Likharev, *Appl. Phys. Lett.* **71**, 3661 (1997).

[3] Y. Naveh and K. Likharev, *Superlattices and Microstructures* **27**, No. 1 (2000).

[4] W. Brown and J. Brewer, eds. *Nonvolatile Semiconductor Memory Technology*, New York: IEEE Press, 1998.

[5] K. Likharev, *Appl. Phys. Lett.* **73**, 2137 (1998).

[6] A. Korotkov and K. Likharev, in: *Techn. Digest of IEDM'99*, p. 223.

[7] K. Likharev, *Proc. of IEEE* **87**, 606 (1999).

[8] K. Likharev and A. Korotkov, in: *Proc. of 1995 ISDRS*, p. 355.

[9] C. Chen, Y. Nakamura and J. Tsai, *Appl. Phys. Lett.* **71**, 2038 (1997).

[10] A. Korotkov, *New device ideas for terabit-scale digital technologies*, Invited talk E14.03 at the APS March meeting (Minneapolis, MN, March 21, 2000), and to be published.

[11] Notice that in logic circuits such exclusion is problematic due to much higher number of interconnects, affecting feasibility of single-electron logic circuits [7].

[12] A. Korotkov and K. Likharev, in: *Abstr. of Int. Workshop on Computational Electronics (Tempe, AZ, Oct. 1995)*, p. 42.

[13] M. Yoo, T. Fulton, H. Hess, R. Willett, L. Dunklebrger, R. Chichester, L. Pfeiffer and K. West, *Science* **276**, 579 (1997).

[14] K. Likharev and V. Semenov, *IEEE Trans. Appl. Supercond.* **1**, 3 (1991).

[15] K. Likharev, in: H. Weinstock, ed. *Applications of Superconductivity*, Dordrecht: Kluwer, 1999.

[16] K. Likharev, in: S. Luryi, J. Xu and A. Zaslavsky, eds. *Future Trends in Microelectronics*, New York: Wiley, 1999, p. 323.